A SURVEY ON IMAGE SCALING TECHNIQUES

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ABSTRACT:

The paper presents study of image scaling techniques. Image scaling is the process of resizing a digital image. Scaling is a non-trivial process that involves a trade-off between efficiency, smoothness and sharpness. With bitmap graphics, as the size of an image is reduced or enlarged, the pixels that form the image become increasingly visible, making the image appear "soft" if pixels are averaged, or jagged if not. With vector graphics the trade-off may be in processing power for re-rendering the image, which may be noticeable as slow re-rendering with still graphics, or slower frame rate and frame skipping in computer animation.

KEYWORDS: Image scaling, 3D animations, 2D vector animations etc.

(I) INTRODUCTION :

Image scaling is the process of resizing a digital image. Scaling is a non-trivial process that involves a trade-off between efficiency, smoothness and sharpness.
With bitmap graphics, as the size of an image is reduced or enlarged, the pixels that form the image become increasingly visible, making the image appear "soft" if pixels are averaged, or jagged if not. With vector graphics the trade-off may be in processing power for re-rendering the image, which may be noticeable as slow re-rendering with still graphics, or slower frame rate and frame skipping in computer animation.

Computer animation is essentially a digital successor to the stop motion techniques used in traditional animation with 3D models and frame-by-frame animation of 2D illustrations. Computer-generated animations are more controllable than other more physically based processes, such as constructing miniatures for effects shots or hiring extras for crowd scenes, and because it allows the creation of images that would not be feasible using any other technology. It can also allow a single graphic artist to produce such content without the use of actors, expensive set pieces, or props.

For 3D animations, objects (models) are built on the computer monitor (modeled) and 3D figures are rigged with a virtual skeleton. For 2D figure animations, separate objects (illustrations) and separate transparent layers are used with or without a virtual skeleton. Then the limbs, eyes, mouth, clothes, etc. of the figure are moved by the animator on key frames. The differences in appearance between key frames are automatically calculated by the computer in a process known as tweening or morphing. Finally, the animation is rendered.

IMAGE SCALING technique is widely used in the field of digital image processing. In common applications, such as medical image processing, image zooming, computer graphic , online videos , image scaling plays a more and more important role. Today, the image scalar is widely adopted in electric devices, such as portable healthcare devices, electronic measurement

equipment, digital apparatus, digital cameras, digital photo frames, mobile phones, touch panel computers. It has become a significant trend to design a low-cost, high-quality, and high-performance image scalar by the very large scale integration (VLSI) technique for multimedia electric products.

RESIZE IMAGES : Resize is a term too vague and ambiguous, it has no specific meaning until we say what it means. There are three very different ways to "resize" an image, and all three have very different meanings and results.
Crop it - to simply cut away some at the edges, to include less area in the final image. A little like zooming in a little tighter, but done afterwords. Same action as scissors on paper, so to speak, except we can still enlarge our image later, to print on larger paper.

- Cropping tighter can improve the composition by removing empty or uninteresting or distracting side detail that contributes nothing, and draws attention away from the subject.
- Cropping tighter increases the size of the subject in the frame, making it more dominant.

Cropping discards those trimmed pixels, making the image pixel dimensions smaller, but primarily, it changes the scene included, and often the shape too. Different paper sizes (4x6, 5x7, 8x10 inches, are each a different shape - more below in Crop section - therefore we also often crop to make our image shape match the paper shape. Our camera always makes its images of the same one shape (aspect ratio, which is width:height), but our intended use often needs other shape(s), to fit it to the printed paper size or viewing screen size. And frankly, a little cropping often improves the composition of many images, removing distracting or uninteresting blank nothingness around the edges, concentrating the actual subject larger (zooming tighter, so to speak). More detail below, at Cropping.

1. Resample it - to create a new image of different image dimensions (in pixels). Re sampling might for example replace 4000 pixels across with only say 1000 new pixels across, still the same scene view, but a much smaller image. Reasons would be to make an excessive size image smaller, maybe to show it smaller on the video screen, or to send it as email, or to print only 6x4 inches size. The plan is to make the image size more appropriate for a purpose of using it. There is no going back, so do not overwrite the original - this second one should be a copy, with a different file name. Re sampling is not reversible, re sampling smaller discards pixels (detail) in order to be smaller. The smaller copy has enough pixels for the smaller size of course, but less than before. More detail below, at Re sampling.

OK, an example before we get into how to do it. This was a D800 camera image, 36 megapixels, 7360 x 4912 pixel dimensions. To show it here on the web screen (our screens are no more than 2 megapixels size, and many are not even that), it was re sampled to an arbitrary 500x333 pixel size, 0.167 megapixels. And by the way (a different subject), do note that even this small image is still quite enlarged here, because the lens image on the camera sensor was much smaller. Now perhaps about 5 inches wide on some screens here (screens vary), but the FX sensor image was only 1.4 inches wide, a DX sensor image is almost 1 inch wide, and a compact image sensor might be less than 1/4 inch wide. Like film sizes (which are generally small too), that's a considerable enlargement. But here, this example is about other properties, like shape.

(II) TECHNIQUES ON IMAGE SCALING:

(A) VLSI Implementations of Image and Video Multimedia Processing Systems :

This paper give an overview of very large scale integrated (VLSI) implementations of multimedia processing systems is given with particular emphasis on architectures for image and video processing.
Alternative design approaches are discussed for dedicated image and video processing circuits and for programmable multimedia processors.

Current design examples of dedicated and programmable architectures are reviewed, and the techniques employed to improve the performance for multimedia processing are therein identified. Future trends in multimedia processing systems are anticipated with respect to current developments in emerging image and video multimedia applications.

(B) DCT Implementation with Distributed Arithmetic:

This paper presents an efficient method for implementing the Discrete Cosine Transform (DCT) with distributed arithmetic. While conventional approaches use the original DCT algorithm or the even-odd frequency decomposition of the DCT algorithm, the proposed architecture uses the recursive DCT algorithm and requires less area than the conventional approaches, regardless of the memory reduction techniques employed in the ROM Accumulators (RACs).
An efficient architecture for implementing the scaled DCT with distributed arithmetic is also proposed. The new architecture requires even less area while keeping the same structural regularity for an easy VLSI implementation. A comparison of synthesized DCT processors shows that the proposed method reduces the hardware area of regular and scaled DCT processors by 17 percent and 23 percent, respectively, relative to a conventional design. With the row-column decomposition method, the proposed architectures can be easily extended to compute the two-dimensional DCT required in many image compression applications such as HDTV.

(C) VLSI Architecture for SAR Data Compression :

As a step towards a real-time signal aperture radar (SAR) correlator , custom very large scale integration (VLSI) architectures are developed. Considering the extremely short word length of the data, we derive three architectures with massive parallelism in bit space. Unlike frequency methods, no degradation is introduced during convolution. Optimized for time and space, they are highly suited to VLSI implementation, and a small architecture with 80 taps operating at 10 MHz has been built using an FPGA.

(D) A High-Speed VLSI Design and ASIC Implementation for Constructing Euclidean Distance-Based Discrete Voronoi Diagram :

In this paper, we present a new algorithm to construct a discrete Voronoi diagram based on the Euclidean distance metric in a binary image. The algorithm has linear time complexity and is suited to very large scale integration (VLSI) implementation due to the use of local neighborhood calculations on reduced bit-width data. A cellular architecture for construction of the diagram is proposed. The proposed architecture has been implemented in VLSI using 0.35 micron 2-poly3-metal layer complementary metal– oxide–semiconductor technology, and the dimensions of the chip are 3.16 mm 3.16 mm, with the maximum frequency of operation being 50 MHz.

(E) VLSI Implementation of an Edge-Oriented Image Scaling Processor :

Image scaling is a very important technique and has been widely used in many image processing applications. In this paper, we present an edge-oriented area-pixel scaling processor. To achieve the goal of low cost, the area-pixel scaling technique is implemented with a low-complexity VLSI architecture in our design.

A simple edge catching technique is adopted to preserve the image edge features effectively so as to achieve better image quality. Compared with the previous low-complexity techniques, our method performs better in terms of both quantitative evaluation and visual quality. The seven-stage VLSI architecture of our image scaling processor contains 10.4-K gate counts and yields a processing rate of about 200 MHz by using TSMC 0.18- m technology.

(F) A Low-Cost High-Quality Adaptive Scalar for Real-Time Multimedia Applications:

A novel scaling algorithm is proposed for the implementation of 2-D image scalar. The algorithm consists of a bilinear interpolation, a clamp filter, and a sharpening spatial filter. The bilinear interpolation algorithm is selected due to its having low complexity and high quality. The clamp and sharpening spatial filters are added as pre-filters to solve the blurring and aliasing effects produced by bilinear interpolation. Furthermore, an adaptive technology is used to enhance the effects of clamp and sharpening spatial filters. To reduce memory buffers and computing resources for the very large scale integration (VLSI) implementation, the clamp filter and sharpening spatial filters both convoluted by a 3×3 matrix coefficient kernel are combined into a 5×5 combined convolution filter. The bilinear interpolation is simplified by the co-operation and hardware sharing technique to reduce computing resource and hardware costs. The VLSI architecture in this paper can achieve 280 MHz with 9.28-K gate counts, and its chip area is 46 418μm2 synthesized by a 0.13μm CMOS process. Compared with previous techniques, this paper not only reduces gate counts by more than 46.6% and power consumptions by 24.2%, but also improves average quality by over 0.42 dB.

(G) Real-Time Architecture for a Robust Multi-Scale Stereo Engine on FPGA:

In this work, we present a real-time implementation of a stereo algorithm on field-programmable gate array (FPGA). The approach is a phase-based model that allows computation with sub-pixel accuracy. The algorithm uses a robust multi-scale and multi-orientation method that optimizes the estimation extraction with respect to the local image structure support. With respect to the state of the art, our work increases the on-chip power of computation compared to previous approaches in order to obtain a good accuracy of results with a large disparity range. In addition, our approach is specially suited for unconstrained environments applications thanks to the robustness of the phase information, capable of dealing with severe illumination changes and with small affine deformation between the image pair. This work also includes the rectification images circuitry in order to exploit the epi polar constraints on the chip. The dedicated circuit can rectify and process images of VGA resolution at a frame rate of 57 fps. The implementation uses a fine pipelined method (also with superscalar units) and multiple user defined parameters that lead to a high working frequency and a good adaptability to different scenarios. In the paper, we present different results and we compare them with state of the art approaches.

(H) Techniques for Compensating Memory Errors in JPEG2000:

This paper presents novel techniques to mitigate the effects of SRAM memory failures caused by low voltage operation in JPEG2000 implementations. We investigate error control coding schemes , specifically single error correction double error detection code based schemes, and propose an unequal error protection scheme tailored for JPEG2000 that reduces memory overhead with minimal effect in performance. Furthermore, we propose algorithm-specific techniques that exploit the characteristics of the discrete wavelet transform coefficients to identify and remove SRAM errors. These techniques do not require any additional memory, have low circuit overhead, and more importantly, reduce the memory power consumption significantly with only a small reduction in image quality.

(I) Hardware Implementation of a Digital Watermarking System for Video Authentication:

This paper presents a hardware implementation of a digital watermarking system that can insert invisible, semi fragile watermark information into compressed video streams in real time. The watermark embedding is processed in the discrete cosine transform domain. To achieve high performance, the proposed system architecture employs pipeline structure and uses parallelism. Hardware implementation using field programmable gate array has been done, and an experiment was carried out using a custom versatile breadboard for overall performance evaluation.

Experimental results show that a hardware-based video authentication system using this watermarking technique features minimum video quality degradation and can withstand certain potential attacks, i.e., cover-up attacks, cropping, and segment removalon video sequences. Furthermore, the proposed hardware based watermarking system features low power consumption, low cost implementation, high processing speed, and reliability.

(J) VLSI Implementation of a Low-Cost High-Quality Image Scaling Processor :

In this brief, a low-complexity, low-memory requirement, and high-quality algorithm is proposed for VLSI implementation of an image scaling processor. The proposed image scaling algorithm consists of a sharpening spatial filter, a clamp filter, and a bilinear interpolation. To reduce the blurring and aliasing artifacts produced by the bilinear interpolation, the sharpening spatial and clamp filters are added as prefilters. To minimize the memory buffers and computing resources for the proposed image processor design, a T-model and inversed T-model convolution kernels are created for realizing the sharpening spatial and clamp filters.

Furthermore, two T-model or inversed T-model filters are combined into a combined filter which requires only a one-line-buffer memory. Moreover, a reconfigurable calculation unit is invented for decreasing the hardware cost of the combined filter. Moreover, the computing resource and hardware cost of the bilinear interpolator can be efficiently reduced by an algebraic manipulation and hardware sharing techniques. The VLSI architecture in this work can achieve 280 MHz with 6.08-K gate counts, and its core area is 30 378 μm2 synthesized by a 0.13-μm CMOS process. Compared with previous low-complexity techniques, this work reduces gate counts by more than 34.4% and requires only a one-line-buffer memory.

(III) CONCLUSION:

i) Hardware devices for multimedia have to meet the highest processing demands. Moreover, implementation expense has to be competitive with low-cost consumer market devices. Standard processors typically fall short of either aspect.

ii) Embedding the watermark information within high resolution video streams in real time is a challenge.

iii) The architecture is based on the recursive DCT algorithm and requires less hardware than conventional architectures which use the original DCT algorithm or the even-odd frequency decomposition method. An efficient architecture for the scaled DCT with distributed arithmetic

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